Nos. 09/103,623, entitled "HIGH-BANDWIDTH READ AND WRITE ARCHITECTURES FOR NON-VOLATILE MEMORIES", filed June 23, 1998 to Wong et al., 09/128,225, entitled "HIGH DATA RATE WRITE PROCESS FOR NON-VOLATILE FLASH MEMORIES", filed August 3, 1998 to Wong, and 09/086,785, entitled "ANALOG/MULTI-LEVEL MEMORY FOR DIGITAL IMAGING", filed May 28, 1998 to Wong et al., and in commonly-owned U.S. Pat. No. 5,680,341, entitled "PIPELINED RECORD AND PLAYBACK FOR ANALOG NON-VOLATILE MEMORY", filed January 16, 1996, issued October 21, 1997 to Wong et al., all of which are incorporated by reference in their entirety. One pixel of image data with at least 8-bit resolution or at least 256 levels can be stored in each memory storage element in the memory 210.

Please modify the paragraph at page 20, lines 4-23, as follows:

The write circuitry in each pipeline 510 includes row decoder 332, a row line voltage selection circuit 533, column decoder 334, a column line voltage selection circuit 535, sense amplifier circuit 536, sample-and-hold circuits 521 and 522, and multiplexers 523, 524, and 526. (Sample-and-hold circuits 521 and 522 and multiplexers 523, 524, and 526 are involved in both read and write operations.) Multiplexers 523 and 524 are coupled to sample-and-hold circuits 521 and 522 and respectively select trigger signals and input signals for sample-and-hold circuits 521 and 522. For a write operation, multiplexer 523 selects the output signal of the associated flip-flop 344 (also supplied to 528) to trigger both sample-and-hold circuits 521 and 522, and input selection circuit 524 selects and applies signals Vpp and Vvfy to respective input terminals of sample-and-hold circuits 521 and 522. When the output signal from the associated flip-flop 344 transitions, sample-and-hold circuits 521 and 522 sample and store the current voltages of respective write signals Vpp and Vvfy.

Please modify the paragraph at page 25, line 3, to page 26, line 4, as follows:

In a recording operation illustrated in Fig. 6, both programming cycles and verify cycles are one clock cycle of signal SAMPLECLK in duration. To achieve this, the frequency of signal SAMPLECLK and the duration of each programming cycle is selected according to the minimum time required for a verify cycle. Additionally, the starts of programming operations are separated by one clock cycle. For example, pipeline 510-1 starts a first programming cycle at a time 620 in response to the pulse 615 in signal SR1 from timing

circuit 340. During the programming cycle, the signal VCOL1 applied to the selected column line in array 330-1 is at voltage Vw, and charge pump 582 supplies a current I1 that flows through array 330-1. Current I1 falls during the programming cycle in the characteristic fashion of channel hot electron injection. At time 630, selection circuit 535 in pipeline 510-1 switches signal VCOL1 to read voltage Vr for a verify cycle, and current I1 from charge pump 582 through array 330-1 stops. Also at time 630 when pipeline 510-1 starts the verify cycle, pipeline 510-2 starts a programming cycle in response to pulse 625 on SR2. (Similarly, pulse 645 on SRN is between times 640 and 650). Accordingly, pipelines 510-1 and 510-2 never perform programming at the same time. More generally, only odd numbered pipelines perform programming cycles at the same time as pipeline 510-1, and only even numbered pipelines perform programming cycles at the same time as pipeline 510-2. This effectively cuts the peak current as well as the average current drawn from charge pump 582 in half because at most one half of the pipelines 510 simultaneous performing programming. Additionally, since write operations in pipelines 510 start at different times, most of the programming cycles simultaneously being performed draw much less than the peak programming current for the memory cell. Both factors contribute to significantly reducing the peak total current when compared to a parallel programming operations.

Please modify the paragraph at page 26, line 36, to page 27, line 32, as follows:

A timing diagram for such a recording operation is illustrated in Fig. 7, where programming cycles and verify cycles are one and two clock cycles, respectively, of signal SAMPLECLK in duration. For example, pipeline 510-1 starts a first programming cycle at a time 720 in response to the pulse 715, beginning at time 710 after the ENABLE signal 705 goes low, in signal SR1 from timing circuit 340. During the programming cycle, the signal VCOL1 applied to the selected column line in array 330-1 is at voltage Vw, and charge pump 582 supplies a current I1 that flows through array 330-1. Current I1 falls during the programming cycle in the characteristic fashion of channel hot electron injection. At time 730, selection circuit 535 in pipeline 510-1 switches signal VCOL1 to read voltage Vr for a verify cycle, and current I1 from charge pump 582 through array 330-1 stops. Also at time 730 when pipeline 510-1 starts the verify cycle, pipeline 510-2 starts a programming cycle in response to pulse 725 in signal SR2. At time 740, selection circuit 535 in pipeline 510-1 maintains signal VCOL1 at read voltage Vr to keep array 330-1 in the verify cycle and

prevents current I1 from flowing through array 330-1, selection circuit 535 in pipeline 510-2 switches signal VCOL2 to read voltage Vr to start a verify cycle in array 330-2 and stop current I2 from flowing through array 330-2, and selection circuit 535 in pipeline 510-3 starts a programming cycle in response to pulse 735 in signal SR3. At time 750, a programming cycle is started in array 330-1, the verify cycle is maintained in array 330-2, and a verify cycle is started in array 330-3. (Similarly, pulse 765 on SRN is between times 760 and 770.) Accordingly, only one out of three pipelines is performing programming cycles, while the other two out of three pipelines are performing verify cycles.

Please modify the paragraph at page 28, line 30, to page 29, line 7, as follows:

Referring back to Fig. 2, analog interface circuits 220 coupled to the analog/multi-level memory 210 can be used to access the desired stored analog data from memory locations in the memory 210. Analog interface circuits 220 can include a control circuit for selecting, routing, and buffering the data to desired analog destinations (e.g., analog printer 240, analog display 230, removable analog/multi-level memory 280) or to A/D converter 120 for subsequent routing to digital destinations. Analog image data from pre-processing circuitry 115 can also be transferred directly to an analog display or printer for real-time images or directly to A/D converter 120 for conversion to digital data when the system is not in a burst mode, thereby bypassing analog/multi-level memory 210.